The documentation and process conversion measures necessary to comply with this document shall be completed by 12 January 2008.

INCH-POUND

MIL-PRF-19500/394L
12 October 2007
SUPERSEDING
MIL-PRF-19500/394K
10 October 2006

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, POWER SWITCHING,
TYPES: 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, AND 2N5238S,
JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power, high voltage transistors. Four levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500 and two levels of product assurance are provided for each unencapsulated device type.

1.2 Physical dimensions. See figure 1 (TO- 5) and figures 2 and 3 (JANHC and JANKC).

1.3 Maximum ratings unless otherwise specified T_A = +25°C.

Types	P_T (1) T_A = +25°C	P_T (2) T_C = +25°C	$R_{\theta JA}$ (max) (3)	$R_{\theta JC}$ (max) (4)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	T_{STG} and T_J
	W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	°C
2N4150, S	1.0	15	175	10	100	70	10	10	-65 to
2N5237, S	1.0	15	175	10	150	120	10	10	+200
2N5238, S	1.0	15	175	10	200	170	10	10	

(1) For derating see figure 4.
(2) For derating see figure 5.
(3) For thermal impedance curve see figure 6.
(4) For thermal impedance curve see figure 7.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil .

1.4 Primary electrical characteristics unless otherwise specified T_A = +25°C.

	h_{FE2} (1)	h_{FE3} (1)	C_{obo}	$\|h_{fe}\|$	$V_{BE(sat)}$ (1)	$V_{CE(sat)1}$
Limits	I_C = 5 A dc V_{CE} = 5 V dc	I_C = 10 A dc V_{CE} = 5 V dc	I_E = 0 V_{CB} = 10 V dc 100 kHz ≤ f ≤ 1 MHz	I_C = 0.2 A dc V_{CE} = 10 V dc f = 10 MHz	I_C = 5 A dc I_B = 0.5 A dc	I_C = 5 A dc I_B = 0.5 A dc
			pF		V dc	V dc
Min	40	10		1.5		
Max	120		350	7.5	1.5	0.6

(1) Pulsed, (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

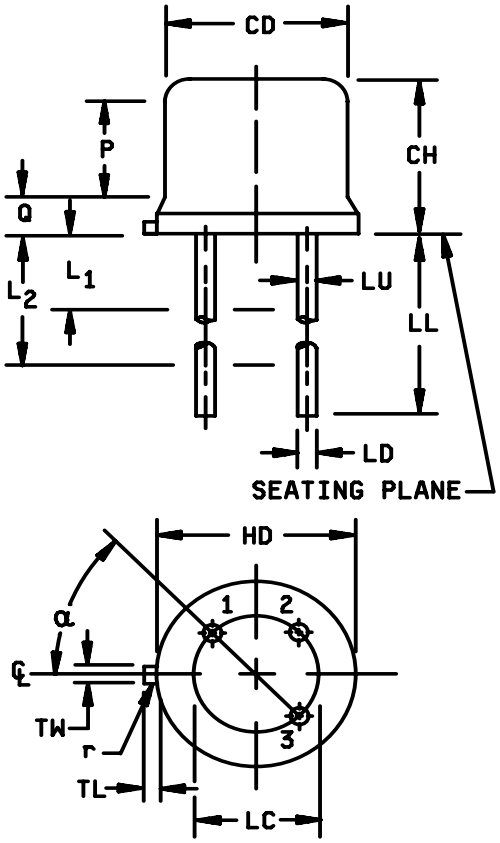
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

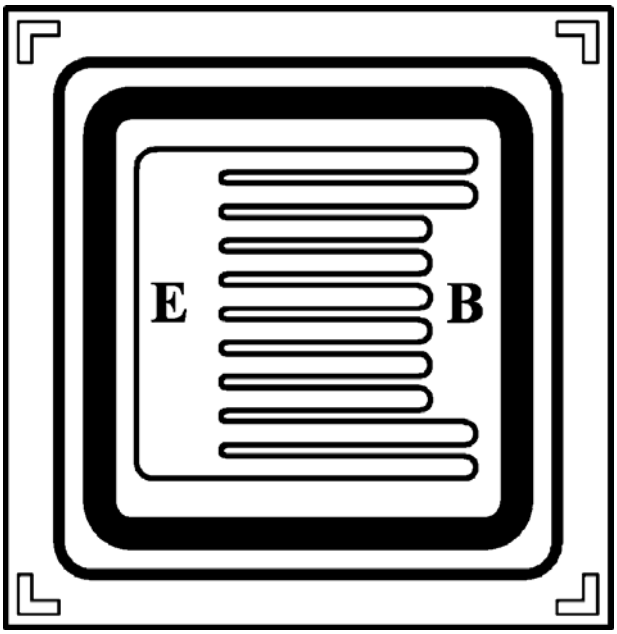
2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Dimensions					
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	See notes				7, 8, 11,12
LU	.016	.019	0.41	0.48	7, 8
L_1		.050		1.27	7, 8
L_2	.250		6.35		7, 8
P	.100		2.54		5
Q		.050		1.27	4
r		.010		0.25	10
TL	.029	.045	0.74	1.14	3
TW	.028	.034	0.71	0.86	2
α	45°TP		45°TP		6



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. For 2N4150, 2N5237, and 2N5238 dimension LL shall be 1.5 inches (38.1 mm) minimum and 1.75 inches (44.4 mm) maximum.
12. For 2N4150S, 2N5237S, and 2N5238S, dimension LL shall be .5 inch (12.7 mm) minimum and .75 inch (19.0 mm) maximum.
13. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
14. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

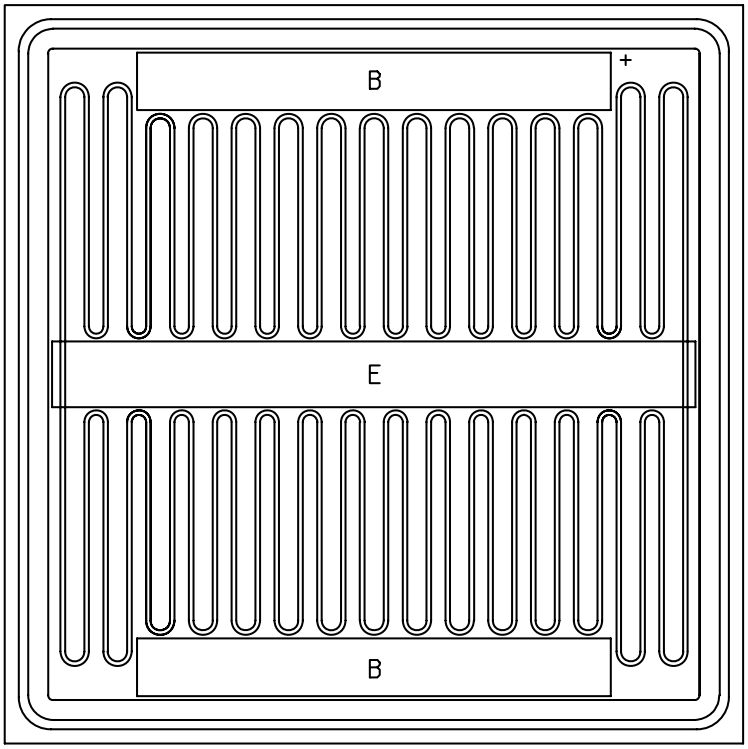
FIGURE 1. Physical dimensions (TO-5).



NOTES:

1. Chip size: .128 x .128 inch ±.002 inch (3.25 x 3.25 ±0.051 mm).
2. Chip thickness: .010 ±.002 inch (0.254 ±0.0381 mm) nominal.
3. Top metal: Aluminum 30,000Å minimum, 33,000Å nominal.
4. Back metal: Gold 3,500Å minimum, 5,000Å nominal.
5. Backside: Collector.
6. Bonding pad: B = .052 x .012 inch (1.321 x 0.305 mm), E = .084 x .012 inch (2.134 x 0.305 mm).

* FIGURE 2. JANHC and JANKC A-version die dimensions.



NOTES:
1. Die size: .155 x .155 inch (3.937 x 3.937 mm).
2. Die thickness: .008 ±.0016 inch (0.2032 ±0.04064 mm).
3. Base pad: .012 x .090 inch (0.3048 x 2.286 mm).
4. Emitter pad: .012 x .090 inch.
5. Back metal: Gold, 2,400 ±720 Å.
6. Top metal: Aluminum, 37,500 ±7,500 Å.
7. Back side: Collector.
8. Glassivation: SiO_2, 7,500 ± 1,500 Ang.

FIGURE 3. JANHC and JANKC B-version die dimensions.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

PCB	Printed circuit board.
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-5) and on figures 2 and 3 (JANHC and JANKC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Construction. These devices shall be constructed in a manner and using materials which enable the devices to meet the applicable requirements of MIL-PRF-19500 and this document.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.3 Screening (JANS, JANTXV, and JANTX levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750, (see 4.3.3).	Thermal impedance, method 3131 of MIL-STD-750, (see 4.3.3).
9	I_{CBO2} and h_{FE1}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CBO2}; h_{FE1}; ΔI_{CB02} = 100 percent of initial value or 50 nA dc, whichever is greater; Δh_{FE1} = ±15 percent of initial value.	I_{CBO2} and h_{FE1}
12	See 4.3.2	See 4.3.2
13	Subgroups 2 and 3 of table I herein; ΔI_{CB02} = 100 percent of initial value or 50 nA dc, whichever is greater; Δh_{FE1} = ±15 percent of initial value.	Subgroup 2 of table I herein; ΔI_{CB02} = 100 percent of initial value or 50 nA dc, whichever is greater; Δh_{FE1} = ±15 percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, “Discrete Semiconductor Die/Chip Lot Acceptance”. Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 Vdc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site’s burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). See table II, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein: delta requirements only apply to subgroups B4 and B5. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.2 herein.

4.4.2.1 Group B inspection (JANS), table E-VIa of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 V dc, 2,000 cycles, adjust device current, or power, to achieve a minimum ΔT_J of +100°C.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIa, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a T_J = +225°C minimum.

4.4.2.2 Group B inspection, (JAN, JANJ, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI, (conformance inspection), shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = 10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and 4.4.3.1 (JANS), and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.2 herein, delta measurements apply to subgroup C6.

4.4.3.1 Group C inspection (JANS), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
C6	1026	1,000 hours at V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3, n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of 4.5.2.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 80 V dc	ΔI_{CB02} (1)	100 percent of initial value or 50 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 5 A dc; pulsed see 4.5.1 (see figure 8).	Δh_{FE2} (1)	±20 percent change from initial reading.

(1) Devices which exceed the table I limits for this test shall not be accepted.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Hermetic seal 4/ 6/	1071	n = 22 devices, c = 0				
Fine leak						
Gross leak						
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours, n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036		I_{CBO1}		10	µA dc
2N4150, 2N4150S		V_{CB} = 100 V dc				
2N5237, 2N5237S		V_{CB} = 150 V dc				
2N5238, 2N5238S		V_{CB} = 200 V dc				
Breakdown voltage, collector to emitter	3011	Bias condition D, I_C = 0.1 A dc, pulsed (see 4.5.1).	$V_{(BR)CEO}$			
2N4150, 2N4150S				70		V dc
2N5237, 2N5237S				120		V dc
2N5238, 2N5238S				170		V dc
Emitter to base cutoff current	3061	V_{EB} = 7 V dc	I_{EBO1}		10	µA dc
Collector to emitter cutoff current	3041	Bias condition D	I_{CEO1}			
2N4150, 2N4150S		V_{CE} = 60 V dc			10	µA dc
2N5237, 2N5237S		V_{CE} = 110 V dc			10	µA dc
2N5238, 2N5238S		V_{CE} = 160 V dc			10	µA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Collector to emitter cutoff current	3041	Bias condition A, V_{BE} = 0.5 V dc.	I_{CEX1}			
2N4150, 2N4150S		V_{CE} = 60 V dc			10	µA dc
2N5237, 2N5237S		V_{CE} = 110 V dc			10	µA dc
2N5238, 2N5238S		V_{CE} = 160 V dc			10	µA dc
Emitter to base cutoff current	3061	Bias condition D, V_{EB} = 5 V dc	I_{EBO2}		0.1	µA dc
Collector to base cutoff current	3036	Bias condition D, V_{CB} = 80 V dc	I_{CBO2}		0.1	µA dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 1 A dc, pulsed (see 4.5.1)	h_{FE1}			
2N4150, 2N4150S				50	200	
2N5237, 2N5237S				50	225	
2N5238, 2N5238S				50	225	
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 5 A dc, pulsed (see 4.5.1)	h_{FE2}	40	120	
Collector to emitter voltage (saturated)	3071	I_C = 5 A dc, I_B = 0.5 A dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.6	V dc
Collector to emitter voltage (saturated)	3071	I_C = 10 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		2.5	V dc
Base emitter voltage saturation	3066	Test condition A, I_C = 5 A dc, I_B = 0.5 A dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.5	V dc
Base emitter voltage saturation	3066	Test condition A, I_C = 10 A dc, I_B = 1 A dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.5	V dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 10 A dc, pulsed (see 4.5.1)	h_{FE3}	10		
Subgroup 3						
High temperature operation:		T_A = +150°C				
Collector to emitter cutoff current		Bias condition A, V_{BE} = -0.5 V dc	I_{CEX2}		100	µA dc
2N4150, 2N4150S		V_{CE} = 60 V dc				
2N5237, 2N5237S		V_{CE} = 110 V dc				
2N5238, 2N5238S		V_{CE} = 160 V dc				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 3 – Continued						
Low temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 5 V dc, I_C = 5 A dc, pulsed (see 4.5.1)	h_{FE4}	20		
Subgroup 4						
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 10 V dc, I_C = 0.2 A dc, f = 10 MHz	$\|h_{fe}\|$	1.5	7.5	
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = 5 V dc, I_C = 50 mA dc, f = 1 kHz	h_{fe}			
2N4150, 2N4150S				40	160	
2N5237, 2N5237S				40	160	
2N5238, 2N5238S				40	250	
Open circuit output capacitance	3236	V_{CB} = 10 V dc, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}		350	pF
Pulse response	3251	Test condition A				
Delay time		See figure 9	t_d		50	ns
Rise time		See figure 9	t_r		500	ns
Storage time		See figure 9	t_s		1.5	µs
Fall time		See figure 9	t_f		500	ns
Subgroup 5						
Safe operating area (continuous dc)	3051	T_C = +25°C, t = 1.0 s,				
Test 1		V_{CE} = 40 V dc, I_C = 0.22 A dc				
Test 2		V_{CE} = 70 V dc, I_C = 90 mA dc				
Test 3						
2N5237, 2N5237S only		V_{CE} = 120 V dc, I_C = 15 mA dc				
2N5238, 2N5238S only		V_{CE} = 170 V dc, I_C = 3.5 mA dc				

See footnotes at end of table.

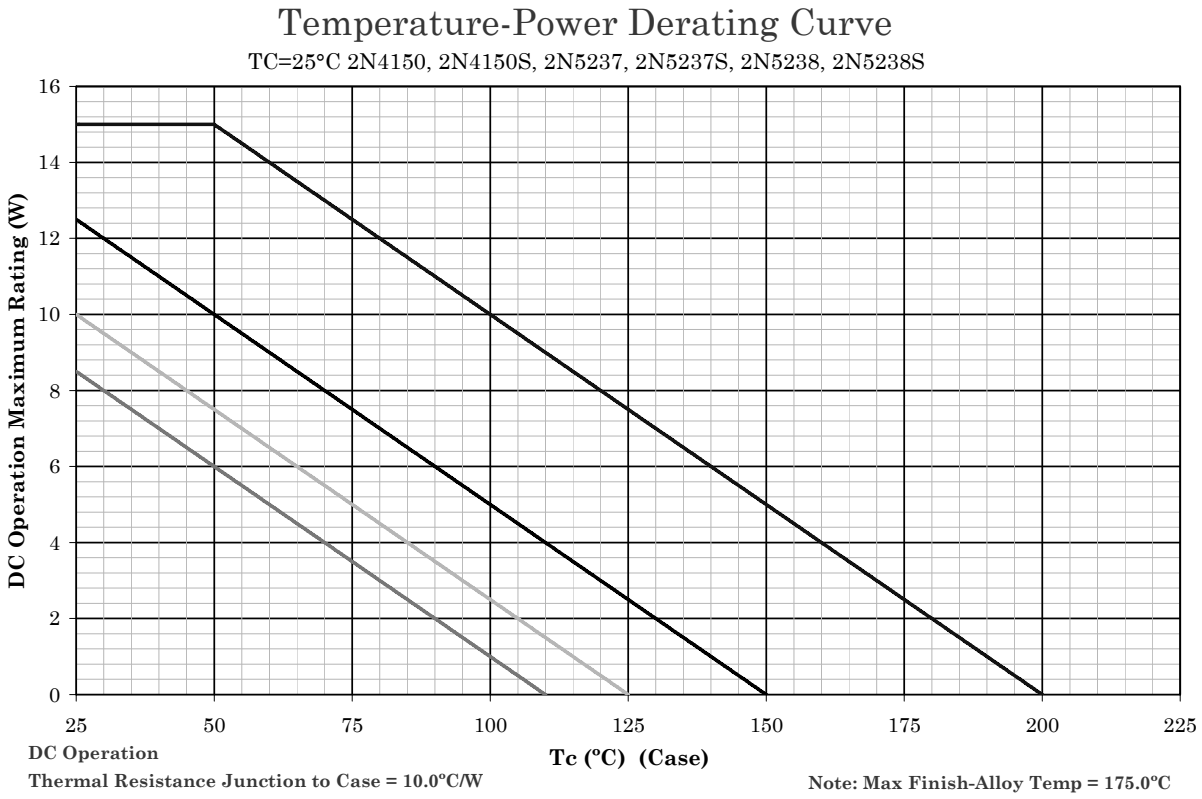
TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 5 - Continued						
Clamped inductive sweep	3053	T_C = +100°C minimum, I_B = 0.5 A dc, I_C = 5 A dc, (see figure 10)				
Electrical measurements		See 4.5.2 herein.				

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 and 4.5.2 herein.	
Subgroup 4			
Thermal impedance curves		See MIL-PRF-19500.	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			3 devices
Electrostatic discharge (ESD)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B	



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 4. Derating for 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S ($R_{\theta JC}$) (TO-5).

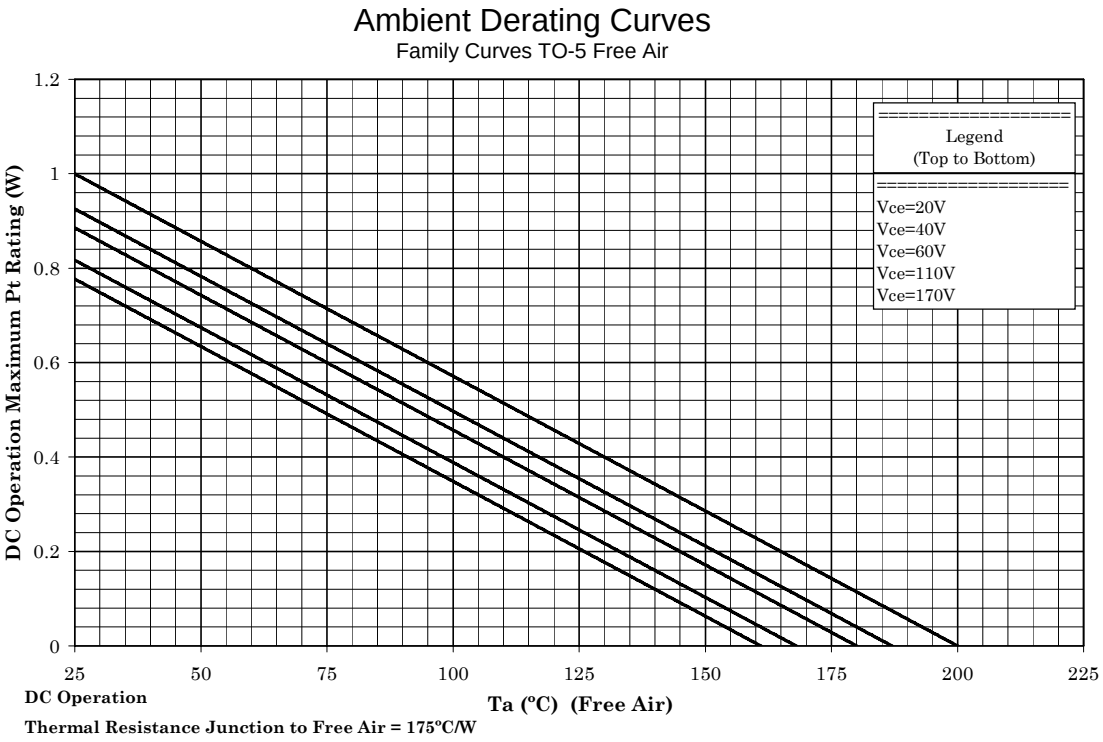
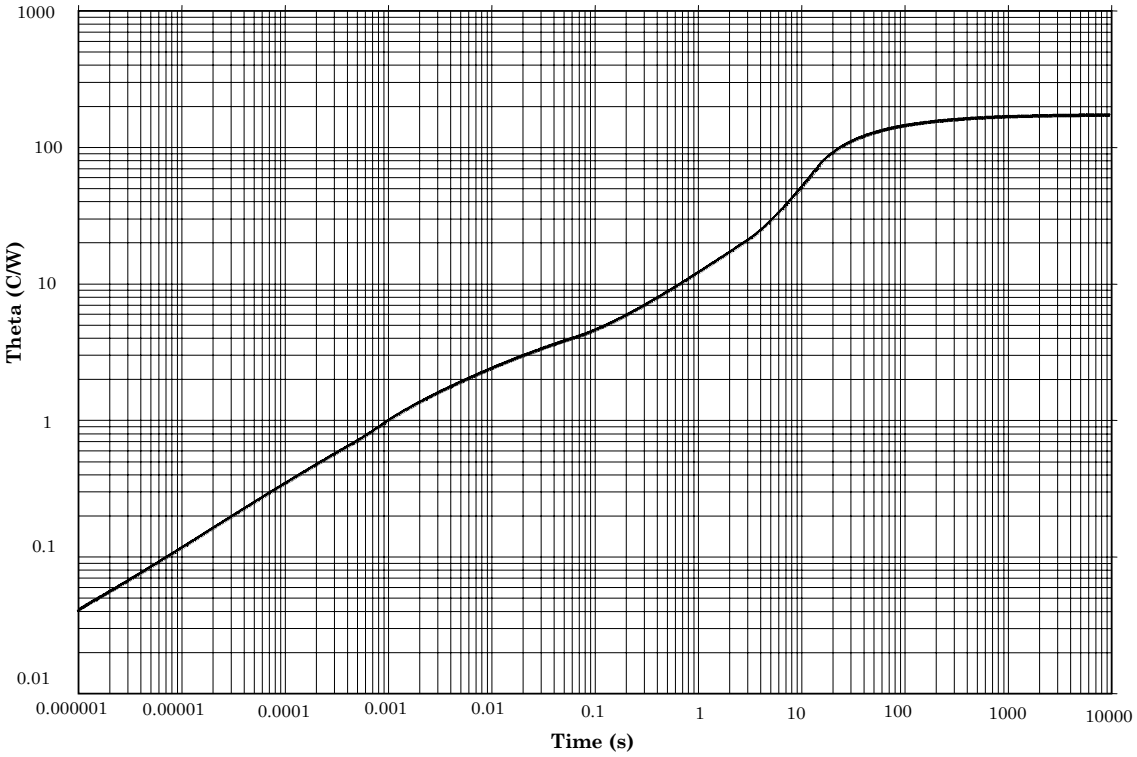


FIGURE 5. Derating for 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S ($R_{\theta JA}$) (TO-5).

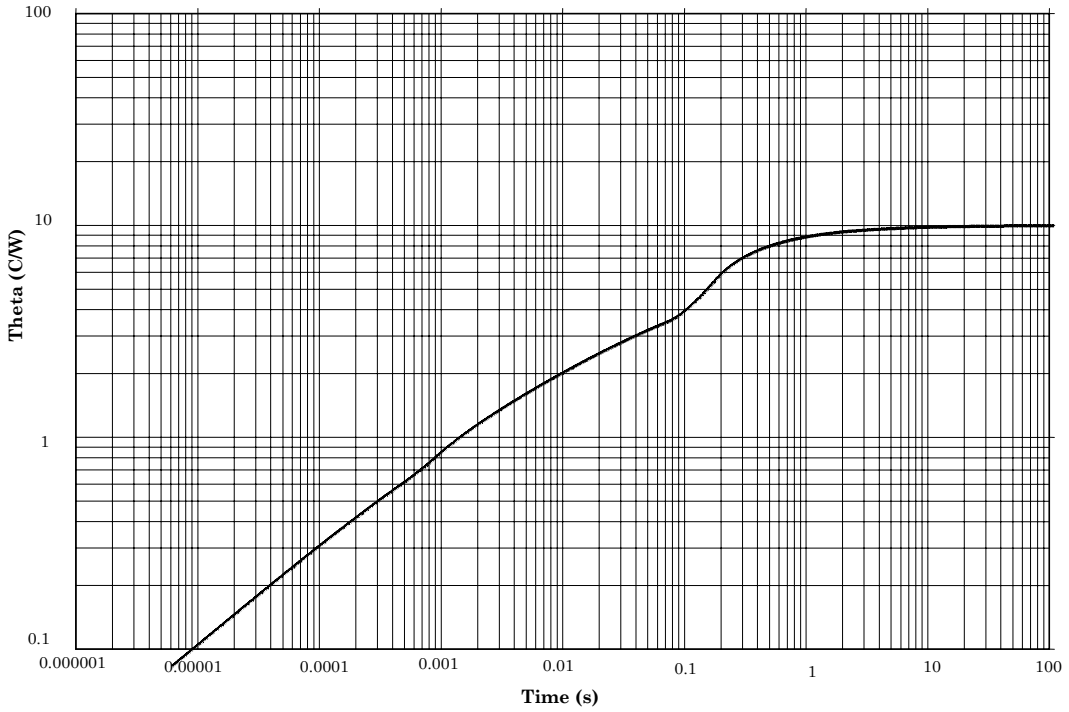
Maximum Thermal Impedance



T_A = +25°C, 1W, thermal resistance $R_{\theta JA}$ = 175°C/W.

FIGURE 6. Thermal impedance graph ($R_{\theta JA}$) for all 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S devices (TO-5).

Maximum Thermal Impedance



T_C = +25°C, thermal resistance $R_{\theta JC}$ = 10°C/W.

FIGURE 7. Thermal impedance graph ($R_{\theta JC}$) for all 2N4150, 2N5237, 2N5238, 2N4150S, 2N5237S, and 2N5238S devices (TO-5) Kovar.

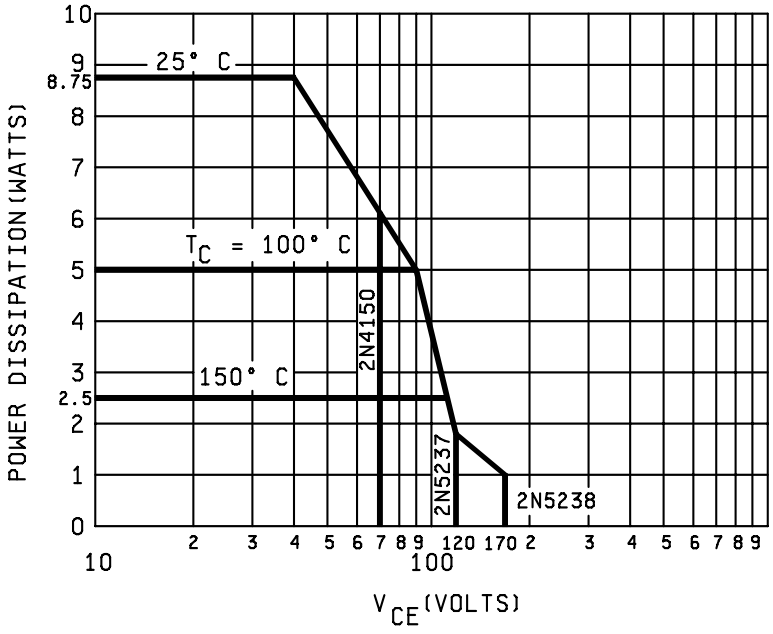


FIGURE 8. Maximum operating conditions - dc forward biased mode.

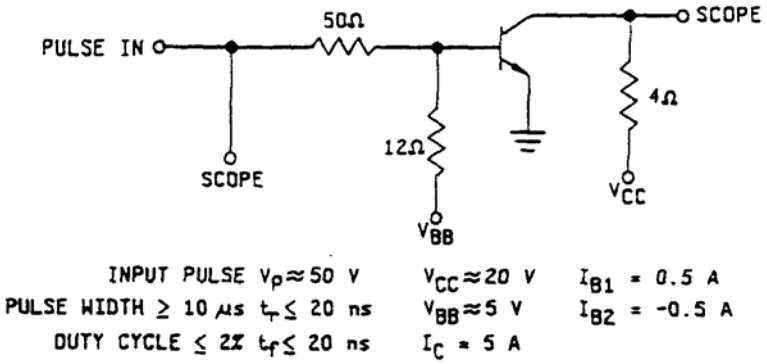
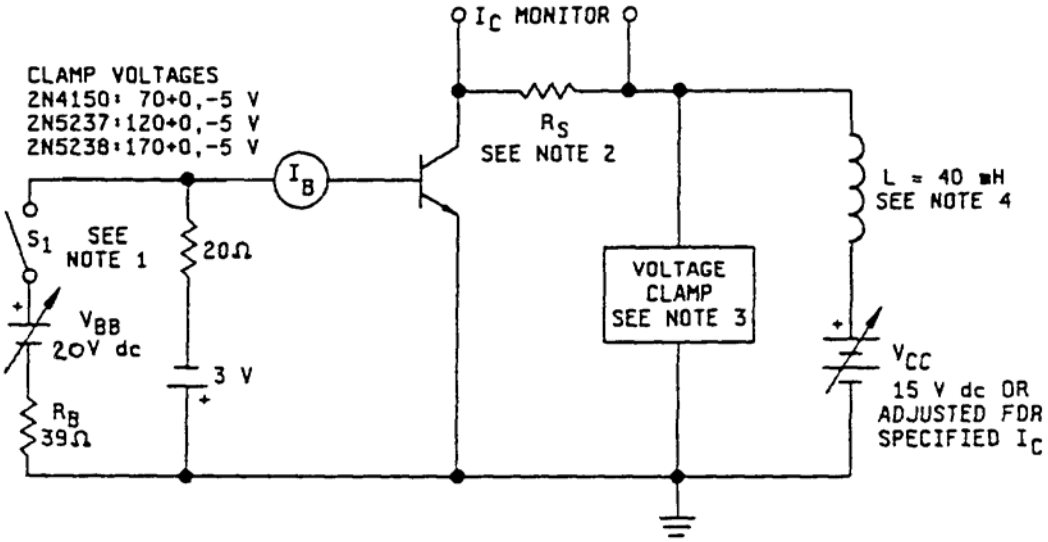


FIGURE 9. Speed of response test circuit.



NOTES:
1. An appropriate pulse generator may be substituted.
2. $R_S \leq 1.0\ \Omega$ noninductive.
3. Clamp voltage: 2N4150: 70 V dc +0 V dc, -5 V dc; 2N5237: 120 V dc +0 V dc, -5 V dc; 2N5238: 170 V dc +0 V dc, -5 V dc.
4. STANCOR C-2691 or equivalent; 2 in series.

FIGURE 10. Clamped inductive sweep test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

6.4 Suppliers of JANHC and JANKC die. The qualified die suppliers with the applicable letter version (example, JANHCA2N4150) will be identified on the QML.

JANHC and JANKC ordering information		
PIN	Manufacturers	
	43611	34156
2N4150	JANHCA2N4150 JANKCA2N4150	JANHCB2N4150 JANKCB2N4150

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
DLA - CC

Review activities:
Army - AR, MI, SM
Air Force - 19, 71, 99

Preparing activity:
DLA - CC

(Project 5961-2007-078)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil .